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Influence of the Amorphous Silicon Thickness on Top Gate Thin-Film Transistor Electrical Performances

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We have analyzed the influence of the hydrogenated amorphous silicon (a-Si:H) thickness on the electrical performances of top gate thin-film transistors (TFTs). We have observed that, when the a-Si:H thickness increases, the threshold voltage and the subthreshold slope decrease. The modification of the TFT apparent field-effect mobility has also been investigated: we have shown that it first increases with the a-Si:H thickness, and then decreases for thicker a-Si:H films. This change of electrical performances is most likely associated with both the variation of a-Si:H microstructure during the film depositions and the effect of parasitic source and drain series resistances. We have demonstrated that for a given TFT geometry, it is therefore possible to define an optimum a-Si:H thickness ensuring maximum TFT electrical performances, and that this optimum thickness increases significantly with the TFT channel length.

KEYWORDS: amorphous silicon, thin-film transistor, top-gate, series resistances, field-effect mobility, field-effect activation energy

1. Introduction and Fabrication Process

The amorphous silicon thin-film transistors (TFTs) used in flat panel display applications can be divided in two categories, depending on the deposition sequence.[1)] The most widely used is the bottom-gate TFT structure, where the film deposition order is as follows: gate metal, gate insulator, amorphous silicon, and phosphorus-doped amorphous silicon. Alternatively, the fabrication order for the top gate structure is as folllows: source and drain contacts, amorphous silicon, gate insulator and finally gate metal. The top gate TFTs have many advantages, among which are:

(i) the top-gate fabrication process allows the use of a very thin a-Si:H layer that can reduce the light-induced TFT leakage current;[1)]
(ii) the gate-line is deposited at the top of the device and can therefore be very thick (no step-coverage concern for a-Si:H and amorphous silicon nitride deposition, which exists in bottom-gate TFT structure). This will reduce the gate-line *RC*-delay in large-area high-resolution active-matrix liquid crystal displays (AMLCDs);[2)]
(iii) A smaller number of photomask steps is usually needed in comparison with the bottom-gate a-Si:H TFTs. This could lower AMLCD production cost.[3)]

It is always assumed that the electrical performances of the top-gate TFTs are lower than those observed for bottom-gate TFTs,[4)] which is the reason for the wider use of the latter structure in AMLCD applications. However, we have recently showed that high-performance top-gate TFTs with electrical performances comparable to bottom-gate TFTs can be fabricated.[5)]

The structure of such a high-performance TFT is shown in Fig. 1. A metal electrode (light shield) was first deposited and patterned on glass substrates, then covered with silicon oxide (a-SiO_x:H). Next, an indium-tin-oxide (ITO) layer was deposited and patterned to form source and drain electrodes and selective phosphorus treatment of the ITO patterned electrodes was done to achieve ohmic source/drain contacts.[6)] Then an intrinsic a-Si:H/a-SiN_x:H bi-layer and a second a-SiN_x:H gate insulator were deposited by plasma-

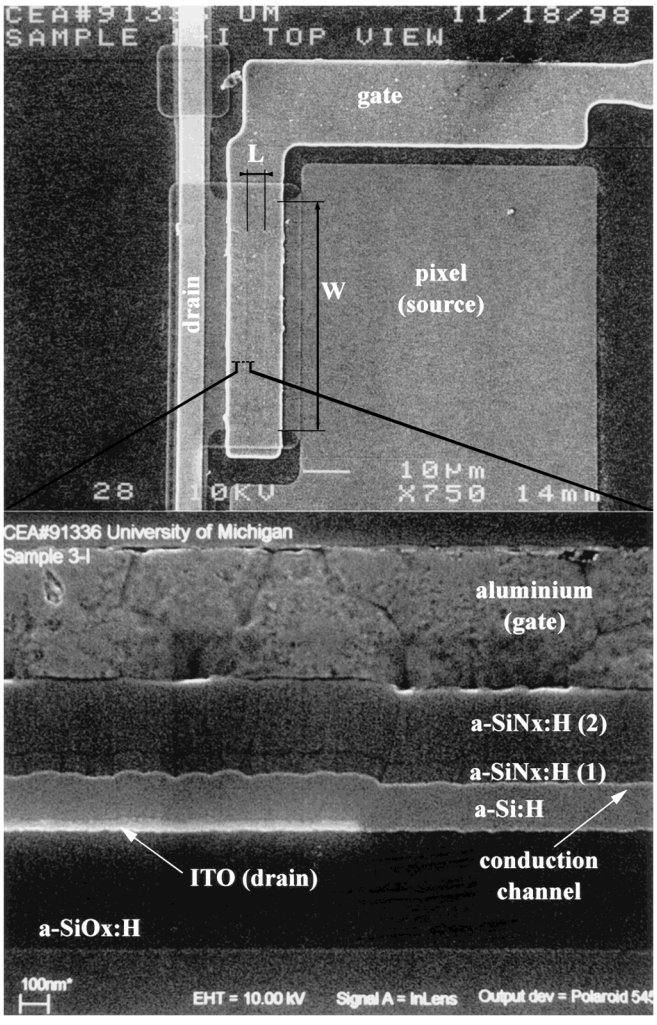

Fig. 1. Scanning electron microscopy (SEM) pictures of the top- and cross-section-views of a typical top-gate a-Si:H TFT structure.

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enhanced chemical vapor deposition (PECVD) at 250°C. Finally, aluminum was deposited and patterned as the TFT gate electrode.

The phosphorus treatment of the source and drain electrodes is a critical step in the TFT fabrication, as it ensures ohmic contacts that are necessary to achieve high-performance devices. Indeed, TFTs fabricated using a similar process, but without the phosphorus treatment, exhibited poor electrical performances and severe current crowding associated with high source and drain series resistances. Secondary ion mass spectrometry (SIMS) analysis of treated ITO electrodes has shown the high selectivity of the phosphine treatment. After treatment, the concentration of phosphorus atoms on the ITO electrodes is more than a decade higher than the concentration of phosphorus atoms on the substrate outside of the ITO electrodes. In addition, we have also used X-ray photoelectron spectroscopy (XPS) to further investigate the effect of the phosphorus treatment and have found out that, most likely, there is formation of InP at the ITO treated surface. These results are consistent with analysis previously performed on similar samples.[7)]

2. a-Si:H TFT Analysis Methods

We have plotted in Fig. 2 the top-gate a-Si:H TFT transfer characteristics in linear regime in a normalized form so that we can accurately compare samples with different geometric parameters and/or different amorphous silicon nitride thicknesses. First, in order to take into account the geometrical dependence of the TFT characteristics, we used the normalized TFT conductance (in Ω^{-1}) instead of the TFT drain current:

$$G = \frac{I_{\mathrm{D}}}{V_{\mathrm{DS}} W/L} \tag{1}$$

where V_{DS} is the drain voltage, W and L the TFT channel width and length, respectively.

Then instead of the gate voltage, we used the electrical charge induced by the gate voltage at the semiconductor/insulator interface (in C/cm^2):

$$Q_{\mathrm{ind}} = V_{\mathrm{G}} \times C_{\mathrm{ins}} \tag{2}$$

where C_{ins} is the insulator capacitance per unit area.

The TFT normalized subthreshold slope S_{norm} was calculated for a fixed value of the TFT conductance ($G = 10^{-10}\,\Omega^{-1}$) and is given by:

$$S_{\mathrm{norm}} = \left(\frac{d\log(I_{\mathrm{D}})}{dQ_{\mathrm{ind}}}\right)^{-1} = C_{\mathrm{ins}}\left(\frac{d\log(I_{\mathrm{D}})}{dV_{\mathrm{G}}}\right)^{-1} \tag{3}$$

In linear regime, i.e. for low drain voltage, the TFT apparent field-effect mobility μ_{FE} and threshold voltage V_{T} or the normalized threshold voltage $V_{\mathrm{T}} \times C_{\mathrm{ins}}$ have been deduced from the following equation, using the MOSFET gradual channel approximation:

$$I_{\mathrm{D}} = \mu_{\mathrm{FE}} C_{\mathrm{ins}} \frac{W}{L}(V_{\mathrm{G}} - V_{\mathrm{T}})V_{\mathrm{DS}}. \tag{4}$$

In such a case, this equation predicts that, for low V_{DS}, a linear I_{D}–V_{G} characteristic can be observed. However, Fig. 3 shows that I_{D}–V_{G} characteristics of TFTs with a very thin or a very thick a-Si:H layer exhibit a non-linear behavior inconsistent with the predictions of the MOSFET gradual channel equation. It has previously been shown[8,9)] that the density-of-states (especially the conduction-band-tail states) present in the amorphous silicon band gap will modify the I_{D}–V_{G} equation as follows: $I_{\mathrm{D}} = \mu_{\mathrm{FE}} C_{\mathrm{ins}} W/L\,(V_{\mathrm{G}} - V_{\mathrm{T}})^{\gamma} V_{\mathrm{DS}}$, where the parameter γ is associated with the density of a-Si:H conduction-band-tail states. However, when using this expression, the unit of the term $\mu_{\mathrm{FE}} C_{\mathrm{ins}} W/L$ is A/V$^{\gamma+1}$ (instead of A/V^2 in the case of the MOSFET-based equation) and consequently depends on the value of γ. Therefore, to ensure proper comparison be-

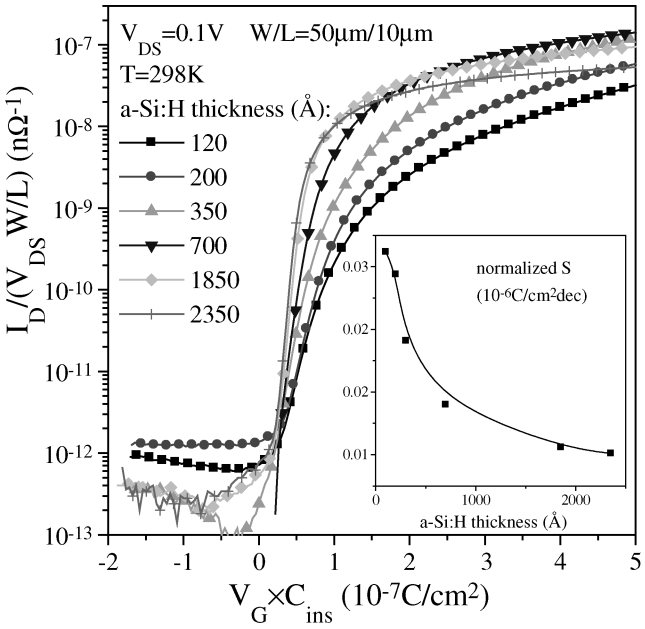

Fig. 2. Transfer characteristics measured in linear regime ($V_{\mathrm{DS}} = 0.1$ V) for 10-μm-long top-gate a-Si:H TFTs with different a-Si:H thicknesses. The corresponding values of the subthreshold slope (normalized to the insulator capacitance) are shown in the inset.

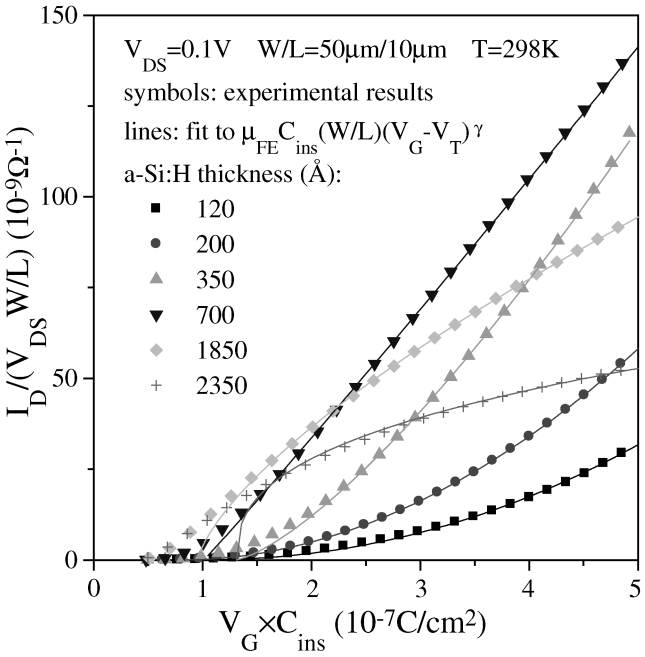

Fig. 3. Transfer characteristics measured in linear regime ($V_{\mathrm{DS}} = 0.1$ V) for 10-μm-long top-gate a-Si:H TFTs with different a-Si:H thicknesses. Symbols show experimental data and solid lines show linear fit to $I_{\mathrm{D}} \propto (V_{\mathrm{G}} - V_{\mathrm{T}})^{\gamma} V_{\mathrm{DS}}$.

tween samples with different γ-values, the TFT field-effect mobility and threshold voltage reported in this paper have been extracted first using the usual MOSFET gradual channel equation. Then, the complete equation describing the I_D–V_G characteristic was used separately for the extraction of the parameter γ.

In addition, the TFT was measured in saturation regime (for $V_{DS} = V_{GS}$), and the saturation field-effect mobility and threshold voltage were extracted from the transfer characteristics using the following equation:

$$I_D = \mu_{FE} C_{ins} \frac{W}{2L} (V_G - V_T)^2. \quad (5)$$

The complete analysis of the TFT electrical performances also involves the extraction of the TFT source and drain series resistances, the intrinsic field-effect mobility and intrinsic threshold voltage. The intrinsic TFT parameters are representative of the electrical characteristics of the conduction channel itself without the influence of the parasitic series resistances. They were extracted by the well-known transmission line method (TLM)[10] using a series of TFTs with different channel lengths measured under a low source-drain voltage, so that we can neglect the space charge limited currents (SCLC) effect.

The total TFT ON resistance is

$$R_T = \frac{V_{DS}}{I_D} = r_{ch} L + R_S + R_D \quad (6)$$

where r_{ch} is the channel resistance per channel length unit, and R_S and R_D are the source and drain series resistances, respectively. Using eqs. (4) and (6), we can express the total TFT ON resistance R_T as a function of the TFT apparent field-effect mobility and threshold voltage.

$$R_T = \frac{L}{\mu_{FE} C_{ins} W (V_G - V_T)} \quad (7)$$

The same equation applied to the ideal TFT (conduction channel) let us express the channel resistance as a function of the intrinsic field-effect mobility and threshold voltage μ_i and V_{Ti} which are representative of the conduction channel material, without the influence of the series resistances:

$$r_{ch} = \frac{1}{\mu_i C_{ins} W (V_G - V_{Ti})}. \quad (8)$$

The extraction of the TFT source and drain series resistances and intrinsic field-effect mobility and threshold voltages is rather straightforward using a series of TFTs with different channel lengths. As illustrated in Fig. 4, we first plot the total ON-resistance as a function of the TFT channel length for different gate voltages ensuring that the TFT is in accumulation regime, then we fit the experimental data to linear curves. This let us obtain the TFT total series resistances ($R_S + R_D$) from the y-intercepts, and the channel resistance per channel length unit (r_{ch}) from the slopes. By plotting the reciprocal of r_{ch} as a function of the gate voltage and, once again, determining its linear fit, the x-intercept gives the intrinsic threshold voltage V_{Ti} and the slope yields to the intrinsic field-effect mobility μ_i as indicated by eq. (8).

The effect of the series resistances can also be partially represented as an increase of the apparent channel: the total TFT

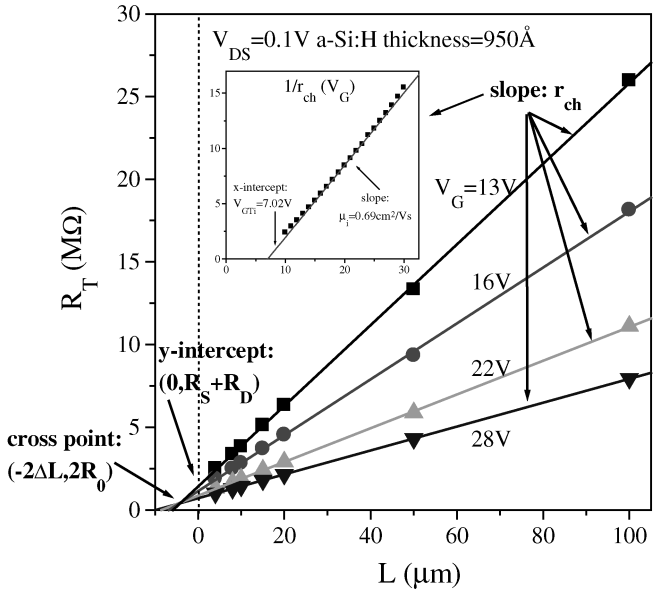

Fig. 4. Illustration of the TLM used to extract the source/drain series resistances and the TFT intrinsic parameters from a series of TFTs with different channel lengths. The total ON resistance R_T has been plotted as a function of the TFT channel length for different gate voltages. Shown in the inset is the evolution of $1/r_{ch}$ with the TFT gate voltage. Symbols: experimental results and solid lines: linear fits.

ON-resistance can be written

$$R_T = \frac{V_{DS}}{I_D} = R_S + R_D + \frac{L}{\mu_i C_{ins} W (V_G - V_{Ti})}$$
$$= 2R_0 + \frac{L + 2\Delta L}{\mu_i C_{ins} W (V_G - V_{Ti})}$$

where ΔL is independent of the gate voltage. R_0 represents the limit of the source and drain series resistance for a very high gate voltage and can therefore be associated with the source and drain contact resistance, while ΔL is associated with the resistance of the access region between the source and drain contacts and the conduction channel.[10] ΔL and R_0 are usually extracted from the R_T versus L curves, as shown in Fig. 4. All the R_T–L curves have a common cross-point located slightly away from the y-axis,[10] which coordinates are ($x = -2\Delta L$, $y = 2R_0$).

The TFT series resistances are closely related to the overlap between source (or drain) contact and gate contact. It has already been shown that the TFT drain current does not usually flow through the whole source or drain contact but is more likely limited to a specific area of the contact.[11–13] More precisely, we can define the TFT characteristic length (L_T) representing the dimension (along the source-drain axis) of the effective contact area, as shown in Fig. 5; this characteristic length increases with the amorphous silicon thickness, the a-Si:H bulk density-of-states, and the source and drain contact resistances.[14] The effective S/D series resistivity r_{Ceff} (in $\Omega \cdot cm^2$) can be defined as the sum of the source (or drain) contact resistivity and the bulk resistivity associated with the access region between the contact and the conduction channel,[13] which is detailed below. The effective S/D series resistivity can be calculated from the S/D contact characteristic length L_T:

$$r_{Ceff} = W L_T^2 r_{ch}. \quad (9)$$

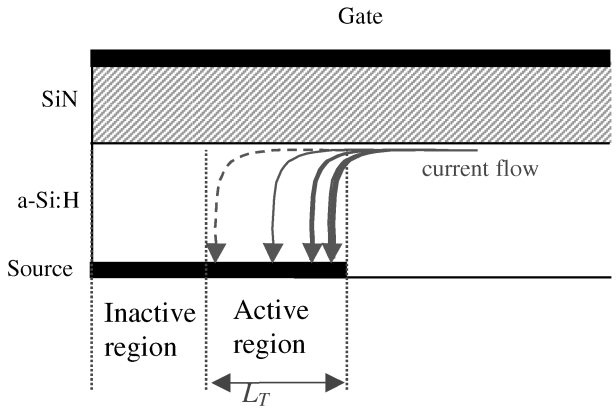

Fig. 5. Definition of the characteristic length L_T at the source/drain contacts.

The S/D contact characteristic length (L_T) is a critical parameter for designing TFTs in display applications. It is clear that, above the L_T-value, the contact dimension (i.e. the overlap between source or drain contact and gate contact) does not have any influence on the parasitic series resistances because the current does not flow through the further part of the source or drain contact (inactive region shown in Fig. 5). On the contrary, below L_T, the whole contact is active regarding to the current flow: the resistance is roughly proportional to the reciprocal of the contact dimension. Therefore, an increase of the contact dimension results in a reduction of the series resistances and an improvement of the TFT electrical performances. However, we have to keep in mind that an increase of the overlap between source or drain contact and gate contact also yields to an increase of the TFT parasitic capacitances that can degrade the display operation. Therefore, the S/D contact characteristic length has to be as small as possible for AMLCD applications.

Regarding the resistivity of the a-Si:H access region, it has been shown that it is closely associated with the band profile in the a-Si:H layer between the source (or drain) contact and the conduction channel[15] and therefore depends strongly on both the a-Si:H thickness and the a-Si:H density-of-states. If the a-Si:H density-of-states were constant throughout the electronic gap, the characteristic length of the band bending (potentials variations) would be the Debye length L_D which can be simply approximated by the following equation:

$$L_D = \sqrt{\frac{\varepsilon_{\text{a-Si:H}}}{q^2 \times \text{density of states}}} \qquad (10)$$

where q is the electron electric charge and $\varepsilon_{\text{a-Si:H}}$ the amorphous silicon permittivity.

However, although the actual a-Si:H density-of-states is not constant throughout the electronic gap, the characteristic length L_D defined by eq. (10) can still be used to describe qualitatively the influence of the a-Si:H thickness and density-of-states on the band profile.

The I_D–V_{DS} characteristics and their derivatives can also be used to evaluate qualitatively the effect of the source and drain series resistances. By plotting the derivative of the I_D–V_{DS} characteristics, we can visualize the existence of the crowding phenomenon that is associated with high source and drain series resistances. Crowding results in an increase of the dI_D/dV_{DS} curve for low V_{DS} values while the absence of crowding yield a monotonous (decreasing) curve.

3. Results and Discussion

We can clearly notice in Figs. 2 and 6 the thickness dependence of the TFT ON-state parameters in linear regime. When the thickness of the amorphous silicon layer increases, we have observed the following changes:

i) Improvement of the subthreshold slope (inset Fig. 2)
ii) Increase of the apparent field-effect mobility for thin a-Si:H layers (Fig. 6)
iii) Reduction of the apparent field-effect mobility for thick a-Si:H layers (Fig. 6)
iv) Increase of the intrinsic field-effect mobility (for all the a-Si:H thicknesses, Fig. 6)
v) Reduction of the threshold voltage (Fig. 6)
vi) Reduction of the coefficient γ (Fig. 7).

The evolutions of the subthreshold slope and the intrinsic field-effect mobility in linear regime suggest that the electronic quality of the amorphous silicon (in terms of density-of-states) is improved, while the reduction of the TFT apparent field-effect mobility observed in case of very thick a-Si:H films results most likely from a stronger influence of the parasitic access resistances. The reduction of the threshold voltage is probably due to a weaker influence of the back interface when the amorphous silicon thickness increases. The decrease of the exponent γ with increasing a-Si:H thickness suggests a lower density of conduction-band-tail states present in thicker a-Si:H films. As shown in Fig. 7, for very thick a-Si:H films and short TFT channel lengths, higher source/drain series resistances result in a low value of γ, i.e. lower than 1.

The results obtained in saturation regime exhibited the same trend than the ones obtained in linear regime: the TFTs made from thicker a-Si:H films have better electrical performances (higher field-effect mobility and lower threshold voltage) than the thinner ones. This is consistent with the idea that the amorphous silicon quality is improved when the film thickness increases.

When the a-Si:H thickness increases, we have also noticed that the influence of the S/D series resistances on the TFT behavior becomes more significant. The evolution of the series resistivity r_{Ceff} with the amorphous silicon thickness is shown in Fig. 8, where we can clearly observe its rapid increase for thick a-Si:H films. In such cases (thick a-Si:H films), the series resistivity r_{Ceff} is most likely associated with the access region between the source (or drain) contact and the conduction channel, the source and drain contact contributions being less significant. For thin a-Si:H layers, the contribution of the access region becomes less significant. However, we can also notice high r_{Ceff}-values for thin a-Si:H films, which could be related to poorer source and drain contacts. However, further investigation is required to clearly identify the origin of the high r_{Ceff}-values extracted from TFTs using thin a-Si:H films.

The TFTs used for display applications have a-Si:H thicknesses in the same range as L_D and the band bending depends strongly on the a-Si:H thickness. The access region resistivity therefore increases very rapidly with the a-Si:H thickness (more than linear dependence),[15] as shown clearly in Fig. 8. Consistently, we can also notice the rapid increase of the characteristic length L_T with the amorphous silicon thick-

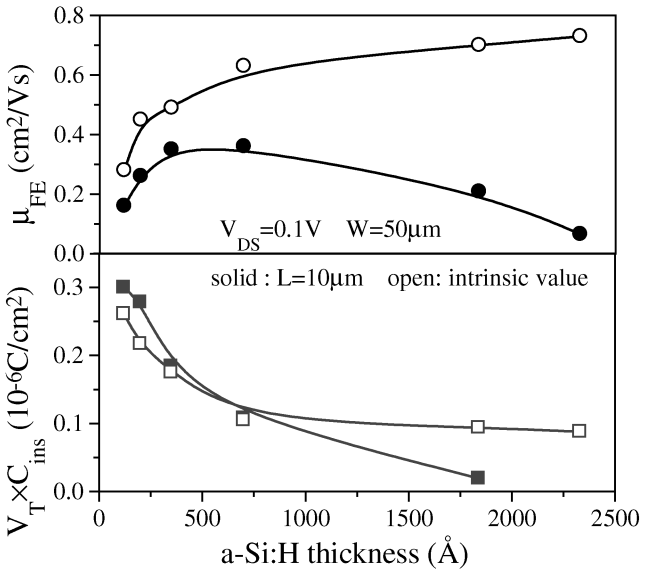

Fig. 6. Variations of the TFT ON-state parameters in linear regime as a function of the a-Si:H thickness. Solid symbols show apparent field-effect mobility and normalized threshold voltage for 10-μm-long TFTs and open symbols show intrinsic field-effect mobility and normalized threshold voltage.

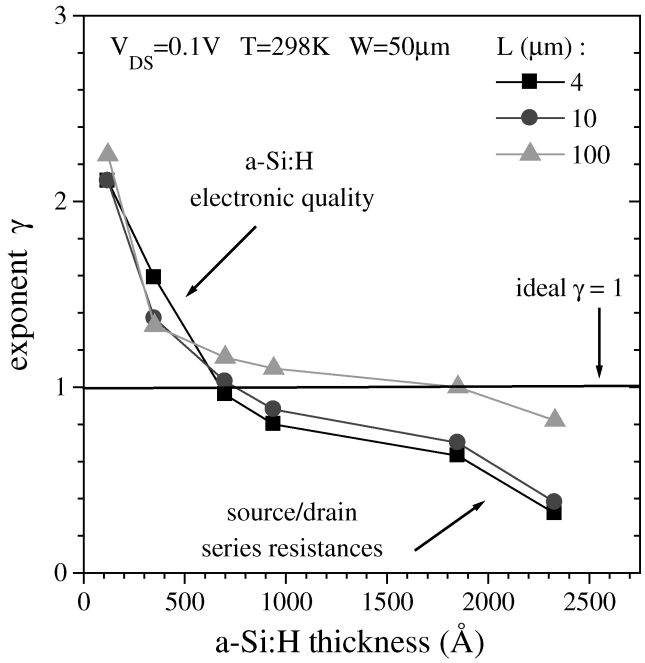

Fig. 7. Exponent γ used to fit the I_D–V_G characteristics shown in Fig. 3 to the equation $I_D = \mu_{FE} C_{ins} W/L (V_G - V_T)^{\gamma} V_{DS}$, as a function of the a-Si:H thickness for different channel lengths.

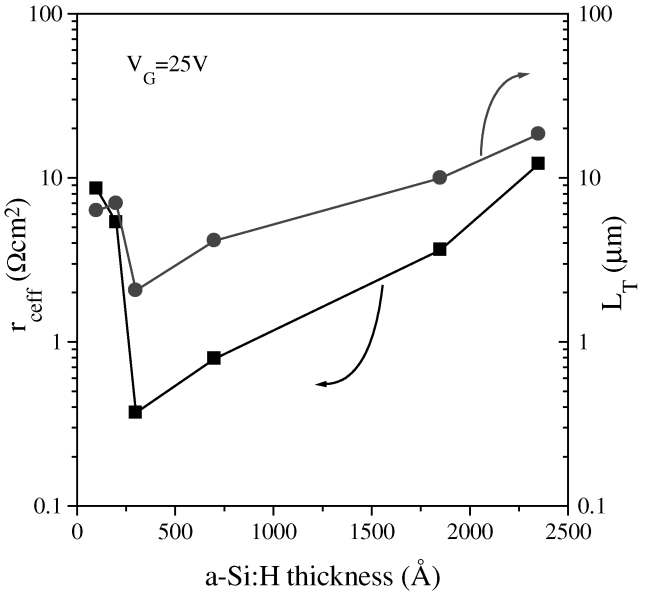

Fig. 8. Influence of the a-Si:H thickness on the source and drain contacts resistivity r_{ceff} and characteristic length L_T (extracted for a gate voltage of 25 V).

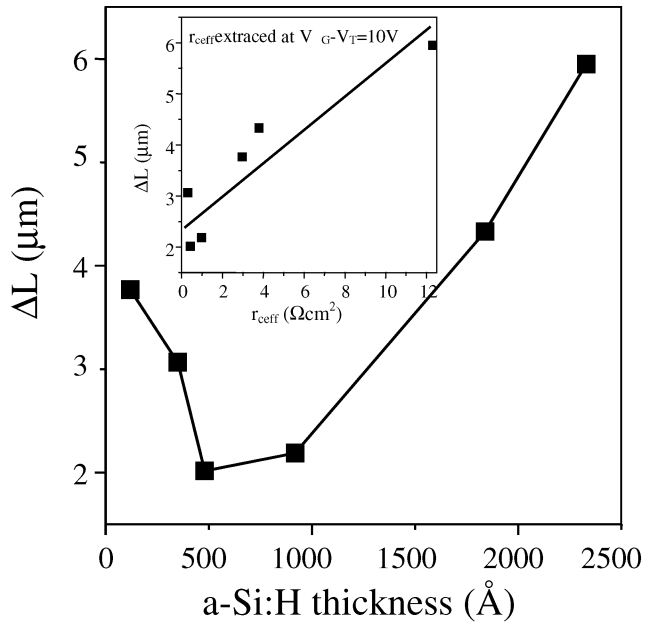

Fig. 9. Evolution of the ΔL-values extracted from Fig. 4 with the a-Si:H thickness. Shown in the inset is the evolution of ΔL-values with the effective series resistivity [extracted from eq. (9)].

ness. Figure 9 shows the evolution of ΔL as a function of the a-Si:H film thickness, very similar to the behavior of the source/drain the series resistivity r_{Ceff}. This is confirmed by the inset plot of ΔL versus r_{Ceff}, showing a clear correlation between these two parameters, which are both associated with the TFT source/drain series resistances.

Figure 10 shows the I_D–V_{DS} characteristics and their derivatives for different a-Si:H thicknesses. We can clearly notice in Fig. 10 the current crowding phenomenon increasing with the a-Si:H film thickness, resulting from the stronger influence of the access resistances in case of thicker a-Si:H films.

These results indicate an inevitable degradation of the TFT electrical performances for very thick a-Si:H layers.

In addition to TFTs, we have also measured top-gate metal-insulator-semiconductor (MIS) capacitors. Figure 11 shows high-frequency (100 kHz) capacitance–voltage (C–V) characteristics of MIS structures with different a-Si:H thicknesses. The curves have been normalized by the insulator capacitance to allow for comparison between samples with different amorphous silicon nitride thicknesses. We can clearly notice a higher degree of C–V stretch-out for the thinner samples, associated with a larger a-Si:H density-of-states. This

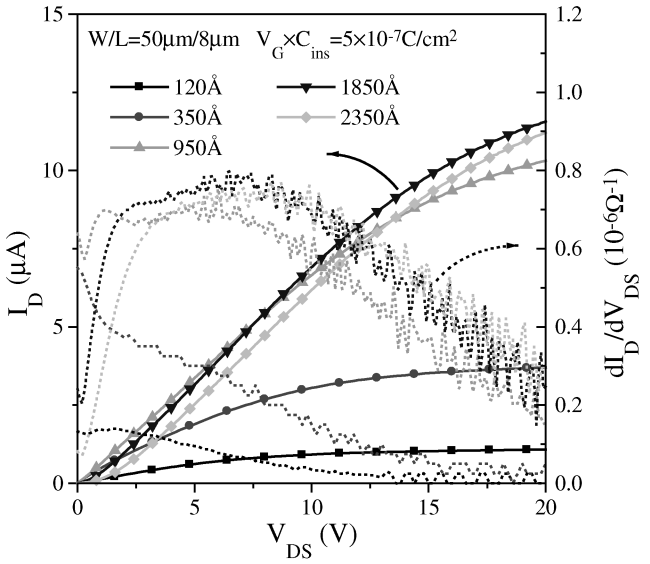

Fig. 10. I_D–V_{DS} (symbols+solid lines) and $dI_D/dV_{DS}-V_{DS}$ (dotted lines) characteristics, for a 8-μm-long top-gate a-Si:H TFT with different a-Si:H thicknesses.

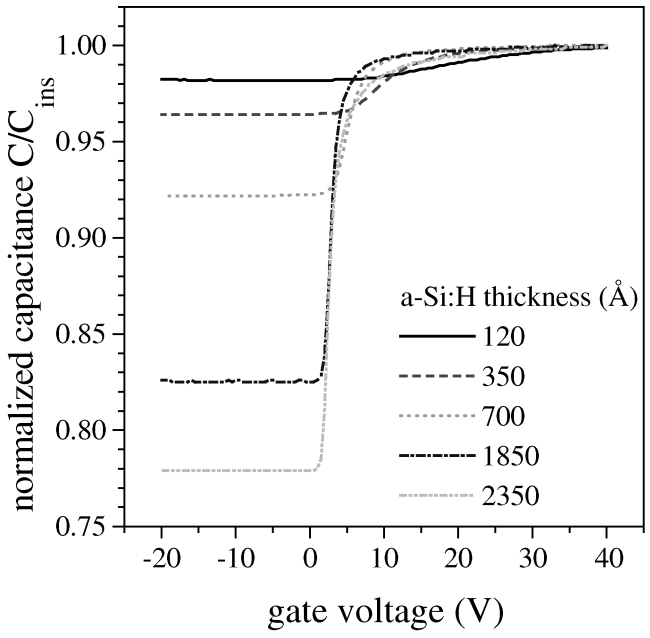

Fig. 11. C–V characteristics measured for top-gate a-Si:H MIS structures with different a-Si:H thicknesses.

observation supports the idea that a-Si:H electronic quality is improved for thicker a-Si:H films.

We have also analyzed the amorphous silicon internal electronic structure by using optical transmission measurements of unpatterned a-Si:H films. Because we were investigating thin films, we had to use specific measurement method to avoid interference fringes that would perturb the spectra.[16] We used a method developed by one of the authors,[17] which utilizes the fact that, at Brewster incidence, the p-polarized light undergoes no reflection at the air/film interface. The following parameters were extracted from the curves plotted in Fig. 12 and are summarized in Table I.

– Tauc band gap energy E_{Tauc}, given by the x-intercept of the linear fit of $\sqrt{\alpha \cdot h\nu}$ versus the photon energy $h\nu$;

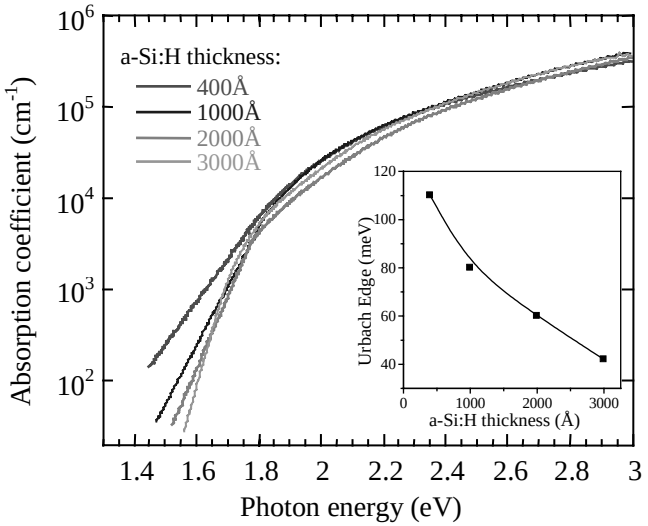

Fig. 12. Absorption coefficient as a function of the incident photon energy, for different a-Si:H thicknesses. Shown in the inset is the evolution of the Urbach edge with the a-Si:H film thickness.

– B-value, the slope of the linear fit of $\sqrt{\alpha \cdot h\nu}$ versus the photon energy $h\nu$;
– E_{04}, the energy corresponding to an absorption coefficient of $10^4\ \text{cm}^{-1}$;
– Urbach Edge, extracted from the slope of the semi-log plot of the absorption versus photon energy curve.

We can notice in Table I a slight increase of the Tauc bandgap and the B-value with the a-Si:H thickness. However, the most significant change observed when the a-Si:H thickness increases is a strong reduction of the Urbach edge (E_0), as seen in the inset of Fig. 12. This is most likely associated with an reduction of the a-Si:H band-tails density-of-states. Such observation is in agreement with the photothermal deflection spectroscopy (PDS)[18] and the electron spin resonance (ESR)[19] measurements, which have indicated that a higher deep-gap state density is expected for thinner a-Si:H films.

In order to supplement the experimental results presented above, we have performed numerical simulation of the a-Si:H TFT behavior, using Semicad Device simulator,[20] a bidimensional simulation program that can describe the TFT behavior. We used the following electronic density-of-states for amorphous silicon: two exponential distributions of band-tail states and two gaussian distributions of monovalent deep-gap states.[21] This program was used to fit the experimental I_D–V_{DS} characteristics for different a-Si:H thicknesses, as shown in Fig. 13. The value of the S/D contact resistance had been set at $0.2\ \Omega\cdot\text{cm}^2$, but had to be adjusted (to $0.5\ \Omega\cdot\text{cm}^2$) in the case of very thick a-Si:H layers: this was needed most likely because the simulation program was not able to take into account the strong influence of the a-Si:H channel access region on the S/D series resistances.

Figure 14 shows the evolution of the values of the conduction-band-tail characteristic energy and deep-gap density-of-states needed to fit the experimental I_D–V_{DS} curves for different a-Si:H thicknesses. We can clearly notice that the amorphous silicon density-of-states (band tail and deep gap) decreases significantly with increasing a-Si:H thickness. This also suggests that the quality of the a-Si:H films in terms of

Table I. Parameters extracted from the absorption curves for different a-Si:H thicknesses.

a-Si:H thickness (Å)	E_{Tauc} (eV)	B ($eV^{-1/2}\,cm^{-1/2}$)	E_{04} (eV)	Urbach edge E_0 (meV)
400	1.69	735	1.85	94
1000	1.70	740	1.87	70
2000	1.82	840	1.91	55
3000	1.82	890	1.88	37

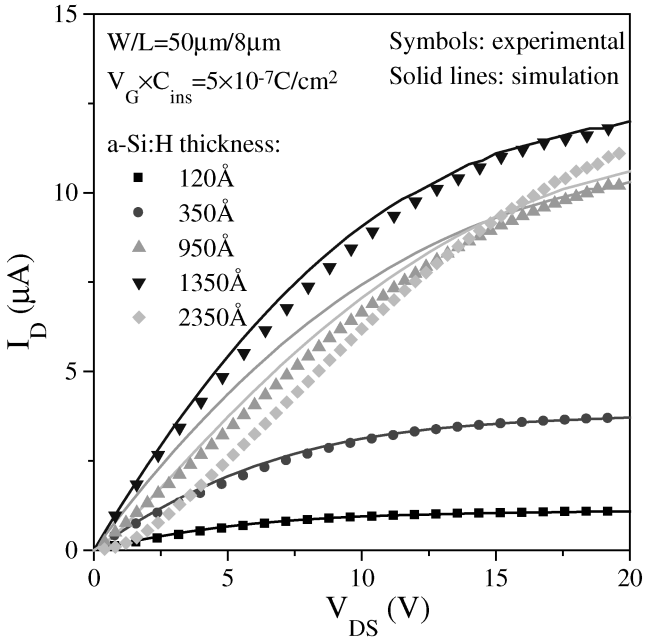

Fig. 13. Example of simulated (solid curves) and experimental (symbols) I_D–V_{DS} characteristics of 8-μm-long a-Si:H TFTs with different a-Si:H thicknesses.

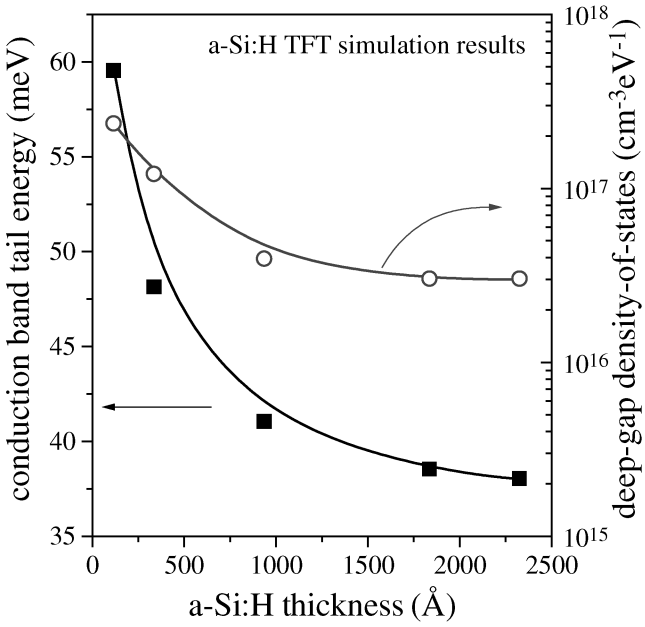

Fig. 14. Values of the conduction band-tail characteristic energy and deep-gap density-of-states used to fit the experimental I_D–V_{DS} characteristics (Fig. 13) as a function of the a-Si:H thickness.

density-of-states is improved for thicker films.

4. Optimum Amorphous Silicon Thickness

As we explained before, the increase of the amorphous silicon thickness first results in an improvement of the TFT electrical performances, due to a better material electronic quality; then, for thicker a-Si:H layers, the access resistances become more and more influent and degrade the TFT electrical performances. Thus, it is necessary to find a compromise regarding the amorphous silicon thickness, which would ensure both a high quality of the material and acceptable values of the parasitic source and drain access resistances. We define an optimum amorphous silicon thickness by the one that results in the highest apparent field-effect mobility (Fig. 15), which depends on the electronic quality of the material and on the TFT source and drain series resistances. Similarly, an optimum value of the a-Si:H thickness can also be defined from the evolution of the TFT field-effect activation energy (E_a) as a function of the film thickness. It is well established that E_a depends on both the a-Si:H electronic quality and the source and drain series resistances (Fig. 16). We have not observed any notable effect of the a-Si:H film thickness on the TFT OFF current in the dark, as shown in Fig. 2. In addition, the TFT structure that we are using includes a light shield at the bottom of the device. The TFTs are consequently not significantly sensitive to light and the amorphous silicon thickness effect on the TFT OFF current can therefore be neglected. We consequently think that the optimum thickness for utilization of the TFT in AMLCDs can be determined from the field-effect mobility or field-effect activation energy. We can see from Figs. 15 and 16 that the TFT field-effect mobility and field-effect activation energy are optimized for concordant values of the a-Si:H thicknesses.

Also, we can notice in Figs. 15 and 16, the clear dependence of the optimum a-Si:H thickness with the TFT channel length, connected to the stronger influence of the source and drain series resistances on shorter channel TFTs. Consequently, in comparison with the long-channel TFTs, the degradation of short-channel TFT electrical performances with increasing a-Si:H thickness clearly appears for thinner a-Si:H layers. Typically, for the devices that we measured, the optimum thickness for a 100 μm-long TFT is above 1000 Å, while the apparent field-effect mobility of a 10 μm-long TFT starts degrading for a-Si:H films thicker than 500 Å. The optimized a-Si:H thickness for short channel TFTs such as the ones used in AMLCDs is below 500 Å, which is comparable to the a-Si:H thickness used for bottom-gate trilayer TFTs, but significantly smaller than the typical amorphous silicon thickness of back-channel etched TFTs.

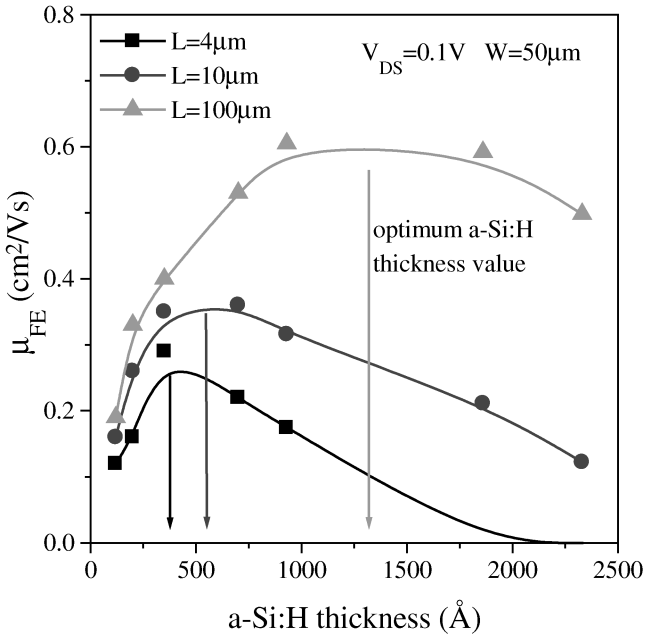

Fig. 15. Variations of the TFT apparent field-effect mobility when the a-Si:H thickness increases for different TFT channel lengths.

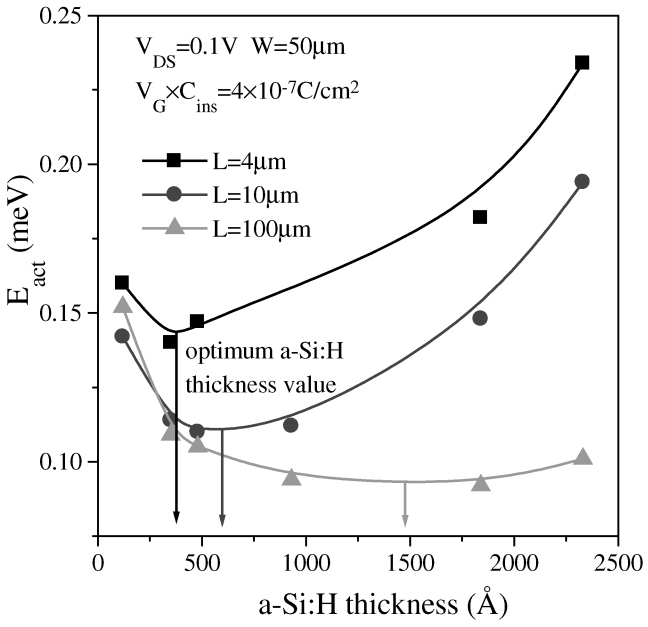

Fig. 16. Variations of the TFT field-effect activation energy when the a-Si:H thickness increases for different TFT channel lengths.

5. Conclusion

In this paper, we have investigated the influence of the a-Si:H thickness on top-gate a-Si:H TFTs electrical performances. When the silicon thickness increases, the main changes are an improvement of the a-Si:H electronic quality and, especially for thick films, a stronger influence of the S/D series resistances. We have demonstrated that for a given TFT geometry it is therefore possible to define an optimum a-Si:H thickness ensuring maximum TFT electrical performances and that this optimum thickness increases significantly with the TFT channel length.

These observations are essential for the future development of large-area high-resolution AMLCDs that will require very short-channel TFTs. Our results have shown that, for such devices, the optimization of the electronic quality of thin amorphous silicon films is critical to achieve a-Si:H TFTs with high electrical performances.

Acknowledgments

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